ESD On-Wafer Characterization: Is TLP Still the Right Measurement Tool?

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***Abstract*—The electrical characterization of devices and circuits regarding their electrostatic discharge (ESD) robustness is done by using several measurement tools. Transmission line pulsing (TLP) and human body model (HBM) testing are the commonly used methods. In this paper, TLP and HBM on-wafer setups are presented regarding their electrical schematics, the type of data that is obtained, and the required calibration methodologies. By using three case studies, both test methods are compared by showing their advantages and disadvantages. It is demonstrated that pulsed measurement methods like TLP testing are not always a suitable tool to fully assess the ESD performance of devices or circuits.**

***Index Terms*—Electrostatic discharges (ESDs), human body model (HBM), tester calibration, transient and waveforms, transmission line pulsing (TLP).**

I. Introduction

THE TRANSFER of electrostatic charges between two objects with different electrostatic potentials occurs when they are brought into close proximity. This event is called electrostatic discharge (ESD), which is a serious threat for the reliability of microelectronic systems and components. Studies have shown that one-third of the failures of modern microelectronic products are caused by ESD [1]. This high amount of losses requires a careful design of protection solutions against ESD-related stress.

Design libraries containing ESD protection elements are developed in the semiconductor industry to provide an ESD protection solution to the circuit designer. These libraries are evaluated on silicon by using the available ESD testing methods. During this evaluation, the robustness of the protection elements against ESD-like stresses is tested to verify their efficiency. After designing a circuit, ESD qualification tests are performed to evaluate the robustness of the final circuit.

On device and circuit levels, several ESD characterization methods for different applications are in use. All the methods are simulating the nature of ESD events. By applying pulsed stresses to a device or circuit under test, its failure level is obtained. The principle of obtaining the failure level of a microelectronic component with pulsed measurements was presented for the first time by Wunsch *et al.* [2]. Since then, several ESD measurement methods have been developed. In this paper, the focus will be on the two most used component-level ESD testing methods. These are transmission line pulsing (TLP) and human body model (HBM) testing.

TLP testing is a pulsed measurement method that uses rectangular pulses as stress. It has been introduced by Maloney and Khurana [3]. It is used to obtain the quasi-static characteristic of a device. The short duration of the TLP pulses prevents the self-heating of devices under stress, which allows reaching a much higher stress level than dc testing. HBM testing is a measurement tool that is used to perform pass–fail measurements. It simulates the event when a human, being charged with a certain voltage, touches a pin of an integrated circuit while another pin of the same circuit is connected to the ground. First introduced as a military standard, HBM testing is used today as an ESD product qualification tool.

In this paper, it is demonstrated that pulsed measurement methods like TLP testing are not always a suitable tool to fully assess the ESD performance of devices or circuits. For many applications, it is needed to study the device behavior in an environment, which is much closer to the ESD events occurring in nature. One of these more realistic ESD characterization methods is HBM. Recently, the authors have shown that by capturing voltage and current waveforms, HBM testers can be used to evaluate the same quasi-static device parameters like in TLP. Additionally, in the same time, the transient behavior of the device is captured [4]. In comparison to TLP, this type of enhanced HBM tester appears as a more powerful evaluation tool for ESD-like stresses.

First, TLP and HBM on-wafer setups are presented regarding their electrical schematics, the type of data that is obtained, and the required calibration methodologies. In the following, both test methods are compared regarding their advantages and disadvantages. The consequences for the characterization process and the interpretation of measurement results are discussed with three case studies.

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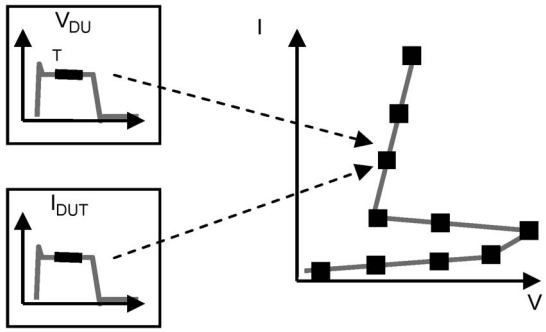

Fig. 1. Measuring TLP IV curve: (left) TLP waveforms and (right) TLP IV curve. V_{DUT}: voltage waveform at DUT. I_{DUT}: current through DUT. V: averaged voltage. I: averaged current.

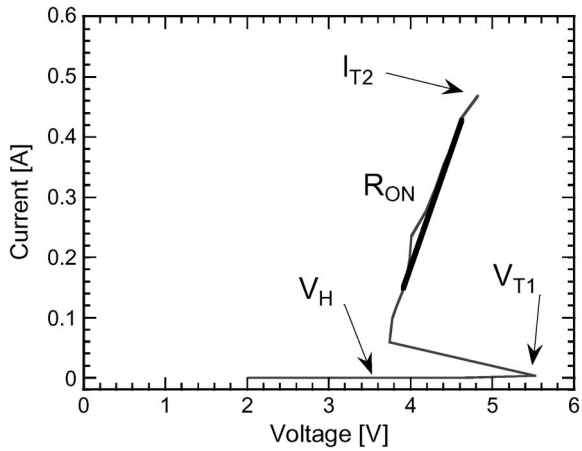

Fig. 2. TLP IV curve with quasi-static device parameters captured from a snap-back device. VT1: turn-ON voltage. VH: holding voltage. RON: ON resistance. IT2: TLP failure level/current.

II. Transmission Line Pulse Testing

TLP testing is performed by discharging a transmission line to a device under test (DUT). The shape of the discharge pulse is rectangular with a user-defined rise time and pulse width. The TLP pulses are usually 100 ns wide and rising within 2 ns. During each pulse, the voltage and current waveforms are captured. In a selected window, which in practice is typically between 70% and 90% of the TLP pulse width, the voltage and current waveforms are averaged. Each averaged voltage and current value forms the measurement points that build the TLP IV curve of a DUT (Fig. 1).

In a TLP IV curve, several characteristic values represent the quasi-static device behavior: turn-ON voltage (VT1), holding voltage (VH), ON-resistance (RON), and TLP failure level (IT2) (Fig. 2). Each value represents parameters that are used as an input for the design of an ESD protection for a certain application.

After each TLP stress, a functional test of the DUT is performed and compared to the functional test taken before TLP testing. Usually, this functional testing is performed by measuring the dc characteristic of the DUT. Stressing the device and performing the functional test are repeated with increased stress level until the device failure current I_{T2} is reached.

The quasi-static device characteristic of a device is accessed by analyzing the IV curve obtained with a TLP tester. Analyzing single TLP waveforms enables the study of the transient

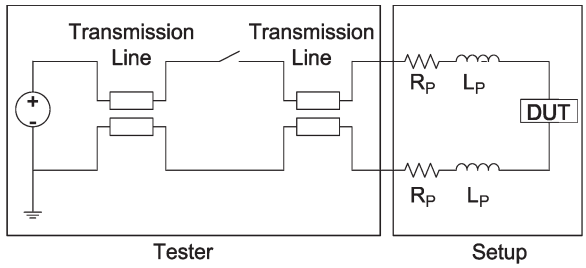

Fig. 3. Schematic of a TLP on-wafer test setup including needle parasitic. R_P: probe needle resistance. L_P: probe needle inductance.

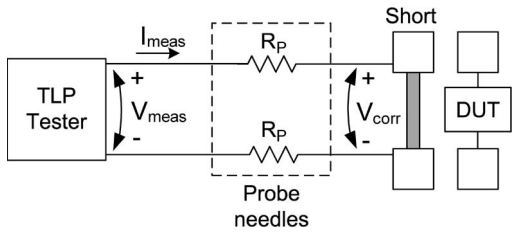

Fig. 4. Schematic of a TLP setup for quasi-static calibration. V_{meas}: measured voltage. I_{meas}: measured current. R_P: probe needle resistance. V_{corr}: corrected "real" voltage.

device behavior under ESD-like stress. For both types of analysis, it is required to fully understand the characteristic of a TLP measurement setup to obtain the right conclusions from the measurement results.

Fig. 3 shows the schematic of an on-wafer TLP setup, which is connected to a DUT. In a TLP setup, parasitic elements exist, which distort the measurement results. Thereby, the probe needles contain the main contributing parasitic elements. The probe parasitic needles are represented by the serial resistance R_P and the serial inductance L_P. The typical values are less than 1 Ω for R_P and less than 100 nH for L_P [5]. In the high-current region of a TLP IV curve, the serial resistance of the needles causes a significant parasitic voltage drop. For the transient analysis of TLP waveforms, L_P is significantly high to distort the waveform data. The influence of both parasitic elements needs to be calibrated out.

Fig. 4 shows the measurement setup for performing a quasi-static calibration that removes parasitic voltage drops caused by the needle resistance. The TLP tester is connected to a short, and the IV curve is measured. The slope of the obtained IV curve gives twice the serial resistance of the probe needles. This resistance is removed from the measurement data obtained from a DUT by using

$$V_{\mathrm{corr}} = V_{\mathrm{meas}} - 2 \cdot R_P \cdot I_{\mathrm{meas}} \tag{1}$$

where V_{corr} is the corrected "real" DUT voltage, V_{meas} is the measured voltage, R_P is the serial resistance of one probe needle, and I_{meas} is the current through the DUT. To use a TLP setup for transient device characterization, the calibration process is more complex [5].

III. HBM Testing

An HBM discharge current (Fig. 5) is flowing through a device or circuit under test, which thereby simulates an ESD stress.

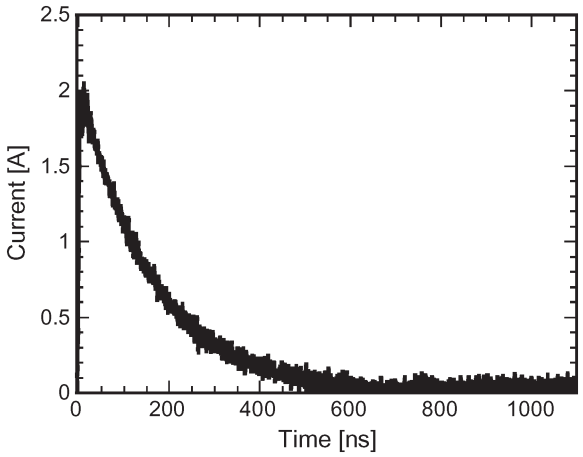

Fig. 5. HBM discharge current for a precharge voltage of 3000 V.

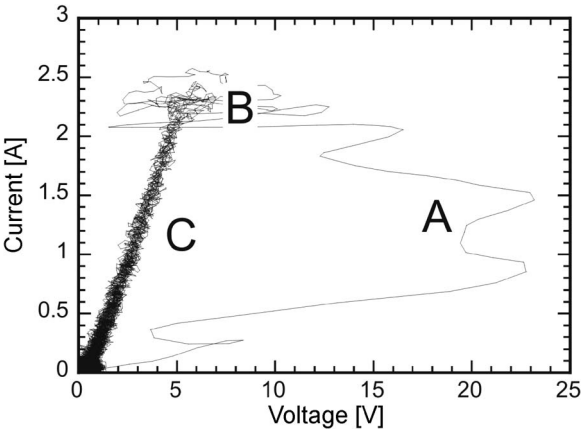

Fig. 6. HBM IV curve obtained from a diode. (A) Overshoot region. (B) Oscillating region. (C) Stable linear region.

The shape of the HBM current pulse is defined in the ESD Association Standard Test Method 5.1. It rises within 2–10 ns and decays during 150 ns. The amplitude of the pulse is defined by the tester precharge voltage divided by 1500-Ω discharge resistance. For a precharge voltage of 1 kV, the corresponding current peak is about 0.66 A.

HBM testers are typically used as a product qualification tool by performing pass–fail measurements. The obtained failure level shows how much ESD-like stress a device is able to withstand. By equipping an HBM tester with a voltage probe and a current transformer, more data can be obtained. With such a setup, the voltage and the current in time during an HBM stress are captured. For each time point of the obtained waveform data, current is plotted over voltage, which thereby forms the HBM IV curve (Fig. 6).

An HBM IV curve reveals three distinct regions: 1) an overshoot part showing the device turn-ON (A); 2) an oscillating part around the peak current (B); and 3) a stable linear part (C) during the falling HBM current. The first two parts show the transient device behavior under ESD stress, whereas the latter represents the quasi-static device behavior. With one HBM pulse, it is possible to simultaneously characterize the transient and quasi-static device behaviors of a device under ESD stress conditions.

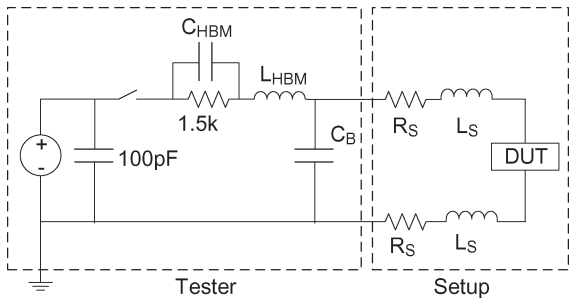

Fig. 7. Schematic of an HBM on-wafer test setup including parasitic. C_{HBM}: parasitic tester capacitance. L_{HBM}: parasitic tester inductance. C_B: board capacitance. R_S: probe needle resistance. L_S: probe needle inductance.

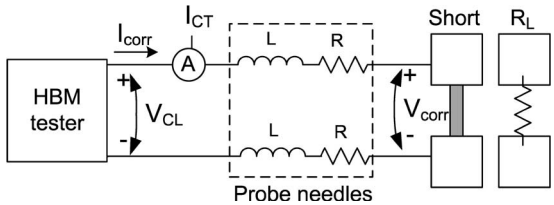

Fig. 8. Setup for HBM calibration. I_{corr}: corrected "real" current. I_{CT}: distorted current measured by current transformer. V_{CL}: measured voltage. V_{corr}: corrected "real" voltage. L_P: parasitic needle inductance. R_P: parasitic needle resistance. R_L: load for calibration.

An HBM tester applies high-current amplitudes in a very short time scale to a DUT. Therefore, each HBM voltage and current measurement is very sensitive to parasitic elements.

Fig. 7 shows the schematic of an HBM on-wafer testing setup, which is connected to a DUT. The tester discharge capacitor, the discharge resistance, and the parasitic elements contributed by the probe needles and the testing setup are shown. These parasitic elements cause an additional voltage drop around the current peak and to the linear region of the HBM IV curve, which need to be calibrated out. The current transformers, which are used to measure the discharge, are usually limited in their bandwidth. Commercially available current transformers, which are suitable for on-wafer HBM measurements, have a bandwidth of between 25 kHz and 2 GHz. The limitation for lower frequencies distorts the measurement of the falling part of the current waveform and needs to be corrected.

Fig. 8 shows the setup that is used to perform the HBM calibration steps [6]. First, the HBM waveforms from a short load and a resistive load R_L (usually 50 Ω) are captured and transformed into the frequency domain. With these data, the transfer function of the current transformer TF and the parasitic impedance of the tester setup Z_P are calculated. The current and voltage waveforms obtained from a DUT are corrected by applying the calibration data to the measurement data in the frequency domain as

$$I_{\mathrm{corr}}(\omega) = \mathrm{TF} \cdot I_{\mathrm{CT}}(\omega) \tag{2}$$

$$V_{\mathrm{corr}}(\omega) = V_{\mathrm{meas}}(\omega) - Z_P \cdot I_{\mathrm{corr}}(\omega) \tag{3}$$

where I_{corr} is the "real" nondistorted current, V_{corr} is the "real" corrected DUT voltage, V_{meas} is the measured voltage, TF is the transfer function of the current transformer, and Z_P is

the parasitic impedance of the measurement setup. An inverse fast Fourier transform of $I_{\rm corr}$ and $V_{\rm corr}$ gives the corrected "real" current and voltage waveforms captured from a DUT. The calibration data are independent of the precharge voltage. A calibration needs to be performed only once before a full set of HBM waveform measurements.

IV. Comparison of TLP and HBM Testing

An HBM tester without having the additions described in the previous section only yields pass–fail measurement data. However, an ESD designer requires a tool that is able verify the design of an ESD protection solution regarding its quasi-static parameters like turn-ON voltage and ON-resistance. For a long time and still ongoing, the TLP testing has been used to fulfill this task. For product qualification purposes, all TLP results regarding device robustness are validated with HBM testing. The use of two different measurement tools for the same task creates the question if the data that are obtained with TLP testing are correlating with the data that is obtained with HBM testing. Several publications have shown that there is a miscorrelation between the HBM and TLP measurement results. It strongly depends on the technology and design of the component under test if the testing results are correlating [7], [8].

A comparison of the TLP and HBM testing setups gives some hints for the observed miscorrelations. In a TLP testing setup, the cables connecting the tester to the DUT are terminated with 50 Ω. With such a setup, the stress on the DUT is not applied by forcing the stress current into the DUT. This excludes the use of a TLP testing system for many applications where a forced current, like it is applied by HBM tester, is needed. The testing of devices with high impedances, like ESD protection elements in the OFF-state or capacitive devices, cannot effectively be performed with TLP testing. The overshoot voltages caused by a delayed turn-ON of devices during an ESD stress are much lower or do not occur during TLP testing. Additionally, TLP with its rectangular pulse shape is a quasi-static measurement tool, whereas HBM applies a transient stress to a DUT. The differences in the testing environment create a different behavior of the DUT. This results in different robustness levels and failure modes.

To demonstrate the capability and the need of HBM on-wafer characterization, three different case studies are demonstrated in the following sections. First, the turn-ON behavior of advanced submicrometer CMOS ESD protection devices is studied. Then, the transient behavior of high-voltage CMOS devices is described, followed by a study of the transient behavior of microelectromechanical system (MEMS) micromirror devices under ESD stress.

V. Case Study I: Turn-on of ESD Protection Elements

With the ongoing scaling in advanced CMOS technologies, the breakdown voltages of the gate oxides of the used transistors are also decreasing. This results in a smaller design window for ESD protection solutions as the maximum turn-ON voltage of an ESD protection device must not be higher than the oxide breakdown voltage of the device, which has to be protected. In this case study, a typical ESD protection device for advanced CMOS circuits, e.g., the silicon-controlled rectifier (SCR), is studied regarding its turn-ON speed and maximum turn-ON voltage.

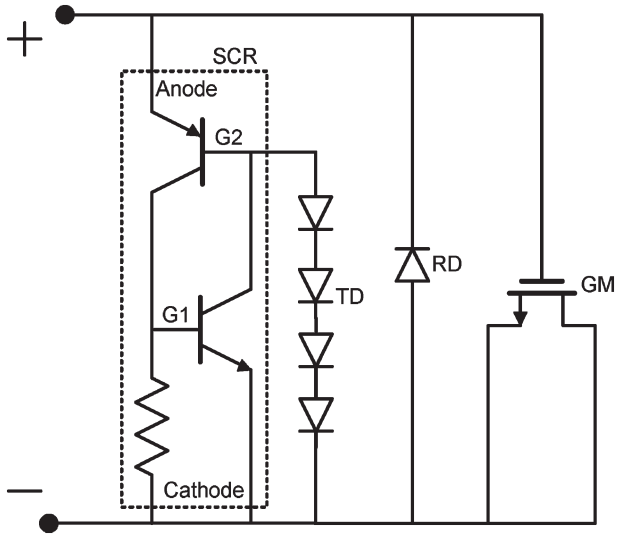

Fig. 9. Schematic of diode-triggered SCR with gate monitor in parallel.

TABLE I
Summary of the Device Types Used in This Paper

	Type A	Type B	Type C
Device	SCR_ref	SCR_all_STI	SCR_all_poly

Fig. 9 shows the schematic of an ESD power clamp consisting of a diode-triggered SCR device [6] and a MOS transistor as gate monitor. Three different SCR variations A, B, and C are used for this study (Table I). Type A is the reference device with small trigger diodes and a small Anode-G2 junction inside the SCR. Type B is a speed-optimized version of Type A, where both the trigger diodes and the Anode-G2 junction are equally wide as the SCR body [9]. A third proposed speed improvement is studied in Type C. The same sizes are kept as in Type B, but both the Anode-G2 junction and the trigger diodes are changed from shallow trench isolation (STI) defined to poly-defined.

TLP measurements are performed on all three SCR types in a standalone configuration without the gate monitor. With the obtained results, it is not possible to distinguish between the different device types. However, when measuring these three types of SCR devices in a configuration with a gate monitor in parallel, the acquired results significantly vary. Measuring the standalone SCR devices with HBM IV indicates the underlying reason: a voltage overshoot is created, which damages the gate oxide of the monitor. These voltage overshoots are limiting the ESD robustness of device types A and B. For device type C, no failure due to oxide breakdown was observed. It fails due to the thermal failure in the SCR, and hence, it yields the same robustness as without the gate monitor.

An overlay of a calibrated HBM IV curve with a calibrated TLP IV curve obtained from the same device shows good correlation (Fig. 10). The holding voltage and the ON-resistance are identical for HBM and TLP.

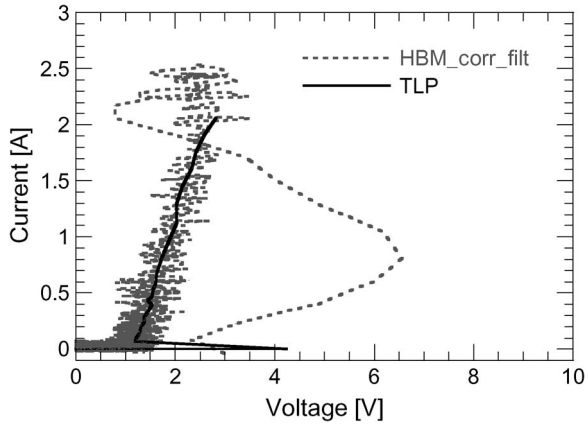

Fig. 10. Overlay of 4-kV HBM IV and TLP IV obtained from device type A.

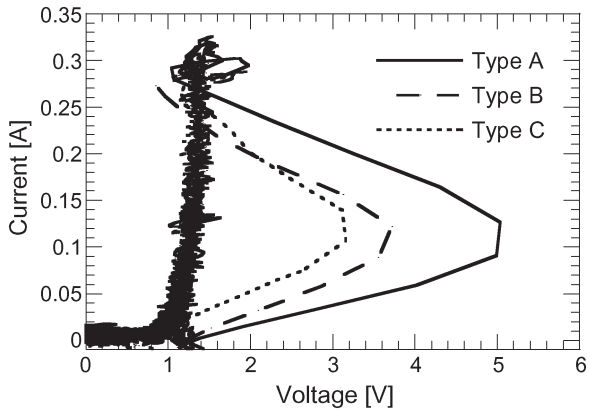

Fig. 11. HBM IV curves obtained from different devices for the same HBM stress level: 500 V.

TABLE II
TLP AND HBM FAILURE LEVELS FOR THE THREE TYPES OF SCR DEVICES WITH A GATE MONITOR IN PARALLEL

	Type A	Type B	Type C
Device	SCR_ref	SCR_all_STI	SCR_all_poly
I_{T2} (A)	0.7	1.45	1.9
HBM (kV)	0.5	2.6	4.6

However, Fig. 11 demonstrates that the different types of SCR devices show a different transient behavior for the same HBM pulse amplitude. Device type A is the slowest device and builds up the highest overshoot voltage during the rising of the HBM pulse. Device type B turns-ON faster than type A. It builds up less overshoot. The highest improvement is obtained by using poly instead of STI for the trigger diodes and inside of the SCR. Device type C builds up the lowest overshoot, which corresponds to the highest turn-ON speed in comparison with types A and B. This leads to an increased HBM robustness when stressing the configuration with the gate monitor in parallel (Table II). Due to the improvements, type C fails at an HBM stress level of 4.6 kV, whereas type B fails at 2.6 kV.

Comparing the transient behavior of the trigger diodes gives more understanding of the different transient behaviors of the SCR devices. Due to their lower base length, poly diodes trigger faster than STI diodes. In poly diodes, the current can flow lateral and does not have to flow underneath the STI. Additionally, the ON-resistance of the poly diode is lower.

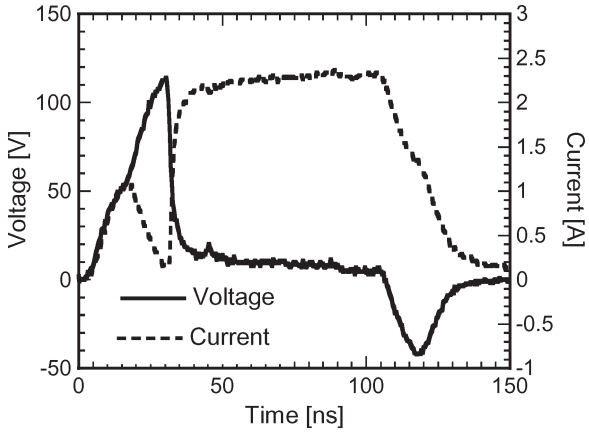

Fig. 12. Calibrated TLP voltage and current waveform obtained from a VDMOS-SCR device (stress level: 2 A).

With this study, it is shown that only TLP testing does not give full insight to the behavior of the studied power clamps under ESD stress. The HBM waveforms have to be captured to evaluate and optimize the ESD performance parameters like turn-ON speed and maximum turn-ON voltage.

VI. CASE STUDY II: TURN-ON OF HIGH-VOLTAGE ESD PROTECTION DEVICES

The microelectronic circuitries in automotive environments are very important, and the amount of applications is increasing. Automotive circuits are usually manufactured in high-voltage technologies. The typical operating voltages are much higher than in standard CMOS technology applications. This requires different ESD protection concepts. Devices manufactured in high-voltage technologies are much larger in size in comparison to low-voltage standard CMOS devices. Due to their dimensions, the transient behavior of high-voltage devices under ESD stress conditions strongly differs. Nonuniform triggering and filamentation effects are occurring [10], [11]. The devices used in this case study are manufactured in a 100-V technology. The devices are stressed with TLP and HBM. With both measurement techniques, the voltage and current waveforms are captured and calibrated using the methods previously described.

Figs. 12 and 13 show the TLP and HBM voltage and current waveforms captured from the same vertical double-diffused MOS SCR (VDMOS-SCR) device. The chosen stress level is similar (about 2 A) for both testing methods.

Comparing the TLP and HBM waveforms visualizes that, during HBM testing, the current and voltage overshoots are occurring, but not during TLP testing. The TLP trigger voltage is about 120 V, whereas in HBM, an overshoot voltage of about 180 V occurs. Additionally, in HBM, a delay between the voltage and current peaks is observed. Through the measured device flows, an HBM current with a peak of around 2.7 A is seen. This is much higher than the nominal expected current of 2 A for 3000 V precharge voltage.

What are the underlying reasons for these results? The different testing environments in TLP and HBM seem to strongly

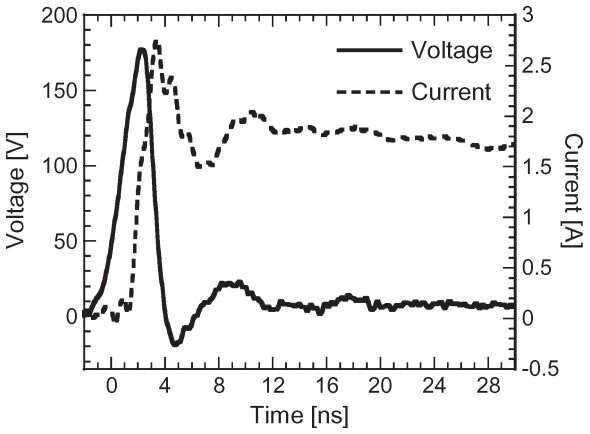

Fig. 13. Calibrated HBM voltage and current waveforms (zoom on device turn-ON) obtained from a VDMOS-SCR device (stress level: 3000 V, which is equivalent to 2A).

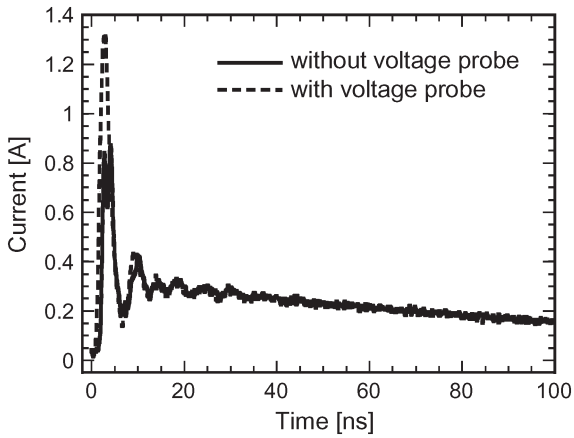

Fig. 15. HBM current waveforms obtained from the same device with and without connected voltage probe (stress level: 500 V, which is equivalent to 0.33 A).

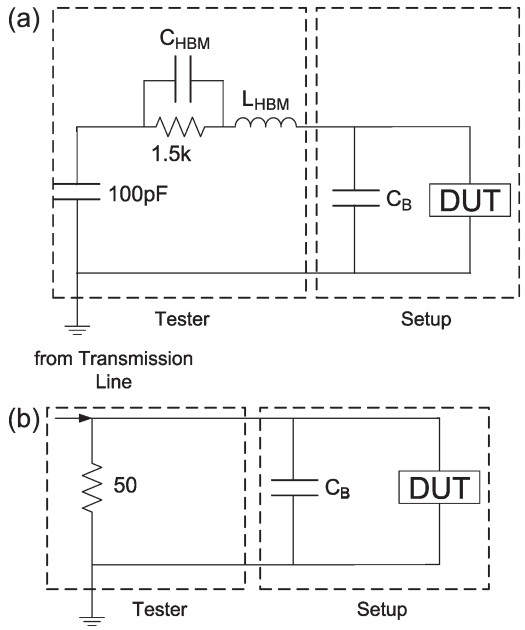

Fig. 14. Equivalent schematic of (a) HBM and (b) TLP setups during device stress. C_{HBM}: parasitic tester capacitance. L_{HBM}: parasitic tester inductance. C_B: board capacitance.

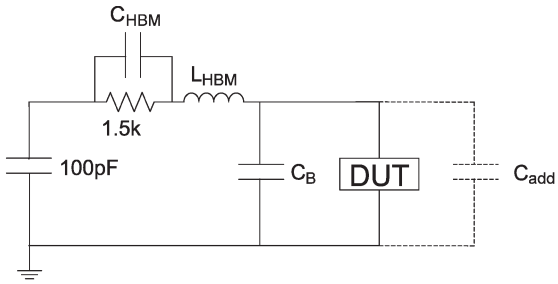

Fig. 16. Schematic of HBM measurement setup with additional capacitor: C_{HBM}–parasitic tester capacitance, L_{HBM}–parasitic tester inductance, C_B–board capacitance, C_{add}–additional capacitor.

influence the transient behavior of the DUT. A comparison between the equivalent schematics for the TLP and HBM setups during the stress of a device gives a better understanding (Fig. 14). In an HBM test setup, the 100-pF discharge capacitor is in parallel to the board capacitance C_B. This results in a much larger equivalent capacitance in parallel to the DUT in the HBM testing setup. The much larger equivalent capacitance in the HBM setup interacts with the DUT and causes the described behavior. Additionally, in the HBM setups, the stress current is forced into the DUT, which creates much higher overshoots during testing.

It is necessary to add a voltage probe to the HBM test setup to measure the voltage. Usually, commercially available voltage probes are able to measure the voltages occurring in an HBM test setup. This type of probe is designed with an input capacitance of 8–10 pF. These values cannot be neglected in relation to the device and board capacitance. Fig. 15 shows how the voltage probe capacitance influences the device trigger behavior. The current overshoot grows from about 0.8 A without a connected voltage probe to 1.4 A with a connected voltage probe.

To study the influence of the capacitive loading of the voltage probe on the HBM waveform measurements, an additional capacitor with different values is placed in parallel to the DUT (Fig. 16).

Values of 6.8 and 22 pF are chosen for the capacitor. The capacitors are used with and without the connected voltage probe to gain more variations. Together with the input capacitance of the voltage probe (8 pF), six different variations are available. With the described setup, an HBM stress is applied to a VDMOS-SCR device. For every capacitance value, the current waveforms have been captured. In case of a connected voltage probe, the voltage waveforms have also been captured. From each waveform, the maximum amplitude is obtained and plotted over the used capacitance value.

Fig. 17 shows maximum voltage and current obtained with an HBM precharge level of 4 kV. As expected, the maximum current increases with increasing additional capacitance. The maximum voltage stays almost constant. The capacitive loading of the voltage probe does not significantly influence the measurement of the voltage overshoot. However, the higher current overshoot due to a higher equivalent capacitance in the measurement setup needs to be taken into account. If a device, like the tested high-voltage device, is used as an ESD protection clamp in a circuit, then the equivalent circuit capacitance reaches similar values like the capacitor values used in this

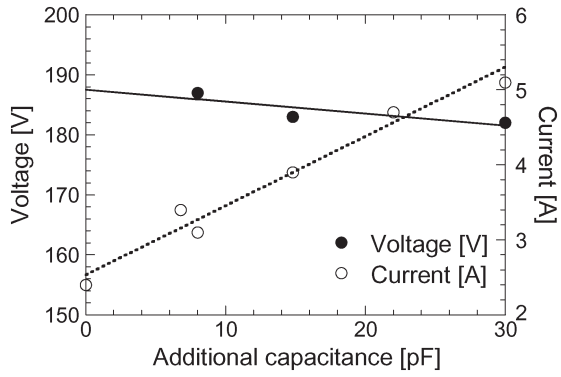

Fig. 17. Maximum voltage and current during an HBM stress on a VD-MOS SCR device, pre-charge voltage: 4kV (equivalent to 2.6A).

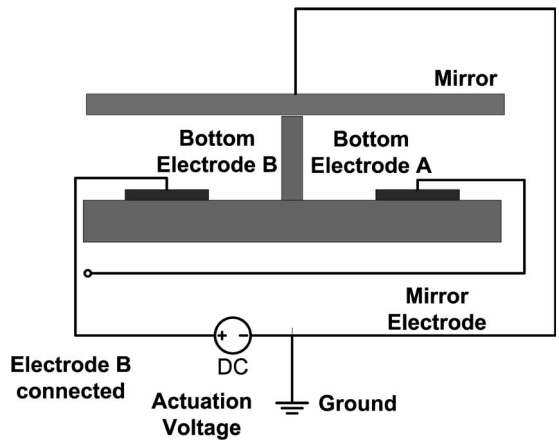

Fig. 18. Schematic diagram of a micro mirror MEMS device (single device).

study. The high current overshoot will occur during an ESD stress and may damage the protected circuit or the surrounding interconnects.

The obtained results have consequences for device characterization under ESD-like stress. TLP as the commonly used characterization method is not a suitable tool to understand the behavior of high-voltage devices under ESD-like stress. The 50-Ω termination of the TLP system does not allow forcing a current into the DUT. These findings are also valid for recently developed 50-Ω HBM testing systems [12]. Such a testing setup prevents a DUT to behave like in a realistic ESD environment. The HBM current waveform is created by applying a filter to a rectangular pulse. The delivery of the pulse is done with a 50-Ω terminated cabling. Such a type of setup is not a suitable tool for the characterization of high-impedance ESD protection devices, as the device is not characterized like with an HBM testing setup.

VII. Case Study III: Characterization of MEMS Devices Under ESD Stress Conditions

MEMS are used in various applications. Due to their wider spread and commercialization, the study of MEMS under ESD-like stress conditions is gaining more interest. To study the behavior of MEMS under ESD stress, micromirror devices (Fig. 18) are stressed with HBM and TLP on-wafer testers. Electrically, these MEMS are capacitors, which change their

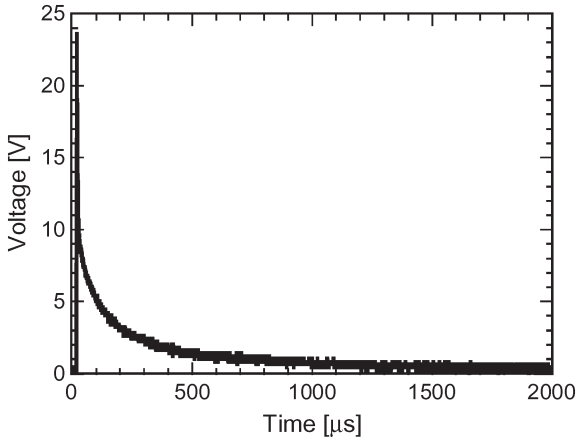

Fig. 19. HBM voltage waveform obtained from a micromirror device (stress level: 30 V).

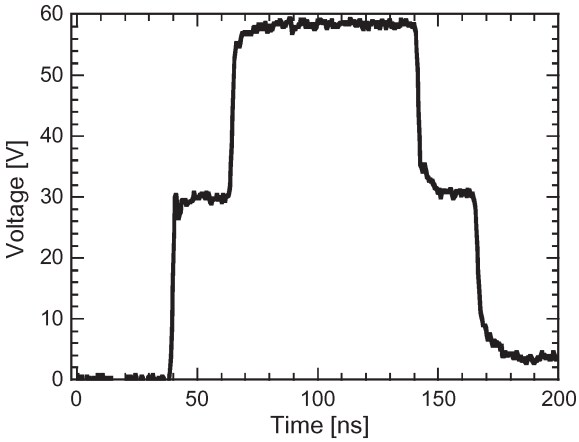

Fig. 20. TLP voltage waveform obtained from a micromirror device (stress level: 30 V).

capacitance with the actuation voltage. To test a mirror device, the ESD stress is applied between the mirror electrode and the ground. As micromirrors are mainly used in an array, the tests are performed in an array configuration. Figs. 19 and 20 show the voltage waveforms obtained with HBM and TLP testing from a micromirror array before device failure.

As expected, the TLP voltage waveform shows a device behavior like an open circuit. As long as the mirror is not pulled in and touching the substrate, an ESD current does not flow. However, the HBM voltage waveform gives more information. About 2 ms after applying the ESD stress, the stored charges in the micromirror are discharged.

Fig. 21 shows the equivalent schematic of a HBM measurement setup connected to a mirror device. In parallel to the mirror capacitance C_{mirror} is the substrate material resistance R_S, which is about 10^{16} Ω. This value is much higher than the parasitic resistance of the HBM measurement setup. The observed waveform shape is attributed to the HBM test setup and not to the mirror device.

However, in the case of "real" ESD stresses, the large substrate resistance of the mirror device strongly influences the transient behavior under ESD stress. The applied charges are not removed fast. The resulting long discharge time after an ESD zap creates an electrical overstress condition, which leads

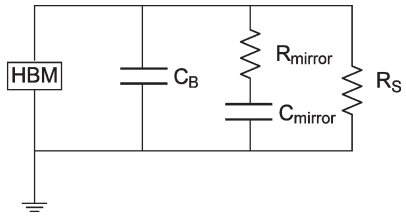

Fig. 21. Equivalent schematic of micro mirror MEMS on a HBM setup. C_B: board capacitance. C_{mirror}: capacitance of mirror device. R_{mirror}: resistance of mirror device. R_S: resistance of substrate material.

to more degradation of MEMS and higher sensitivity to ESD stress [13].

Capacitive devices like micromirror MEMS are not properly characterized with a rectangular pulse measurement method like TLP. The duration of a TLP pulse, which is usually 100 ns long, is much shorter than the decaying time after an HBM stress on the same device. This difference leads to a different transient behavior during TLP testing, which results in an unrealistic stress environment. In comparison, HBM testers allow a characterization in an environment that is close to real ESD stress conditions. The electrical overstress after an ESD stress on the MEMS device is not limited by the shape of the discharge waveform.

VIII. Design of Future ESD Testing Systems

The currently developed ESD Association Human Metal Model (HMM) standard uses a stress current, which is defined in the International Electrotechnical Commission (IEC) 61000-4-2 system-level ESD standard. The purpose of the future HMM standard is to simulate system-level ESD stress conditions on the component and device levels. One main task is the development of a suitable method to deliver the IEC current waveform to a DUT. Among others, one proposed option is the use of a 50-Ω terminated transmission line to deliver the stress pulse. However, applying the findings of the case studies previously presented shows that a 50-Ω terminated HMM system cannot provide a suitable testing environment to characterize components under system-level ESD stress conditions. Such a system does not force the current into the DUT. In contrast, the proposed IEC-conformed ESD gun systems, which are usually used for system-level ESD testing, are the better tool to apply the stress. Similar to HBM testers, they are forcing the ESD current into the DUT, which thereby simulates a realistic ESD stress environment.

IX. Conclusion

Is TLP always the right measurement tool? For many applications, TLP is used to assess the device behavior under ESD stress conditions. With the presented case studies, it has been shown that pulsed measurement methods like TLP testing are not always a suitable tool to fully assess the ESD performance of the device or circuit. The termination in TLP test systems prevents the forcing of a current in the DUT. In nature, there are no ESD environments, which are terminated with 50 Ω. In comparison, the use of HBM on-wafer measurements allows a full characterization of a component under ESD stress conditions, including its quasi-static and transient behavior. The different setup of HBM testers simulates more realistic ESD events than a pulsed measurement method like TLP.

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